



# 64K x 16 Static RAM

## Features

- High speed
  - $t_{AA} = 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 400-mil SOJ

## Functional Description

The WCFS1016C1C is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

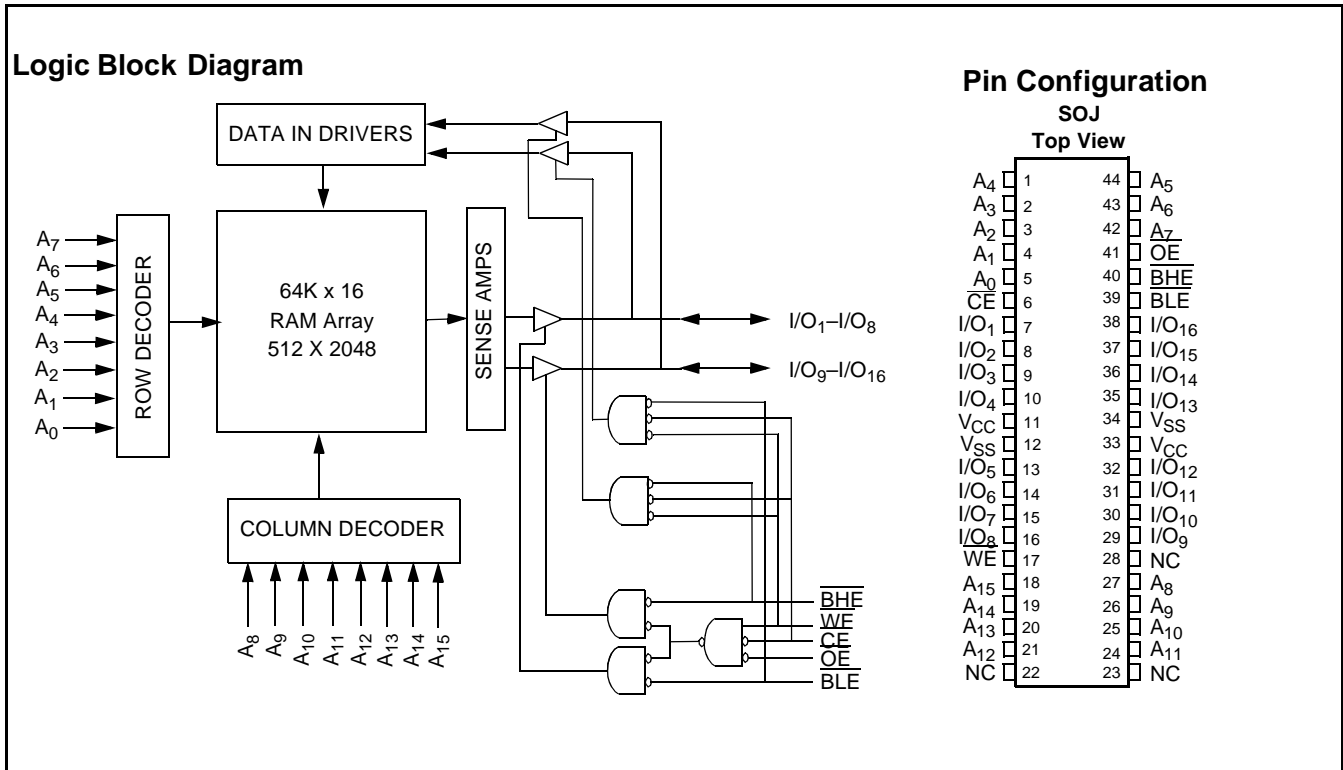
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$

through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The WCFS1016C1C is available in 400-mil-wide SOJ packages.



## Selection Guide

	WCFS1016C1C 12ns	WCFS1016C1C 15ns
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	140	130
Maximum CMOS Standby Current (mA)	10	10



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC}+0.5V$

DC Input Voltage<sup>[1]</sup>..... -0.5V to  $V_{CC}+0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

## Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCFS1016C1C 12ns		WCFS1016C1C 15ns		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC},$ Output Disabled	-1	+1	-1	+1	μA
$I_{OS}$	Output Short Circuit Current <sup>[3]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		140		130	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC},$ $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL},$ $f = f_{MAX}$		40		40	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC},$ $CE \geq$ $V_{CC} - 0.3V, V_{IN} \geq$ $V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V, f = 0$		10		10	mA

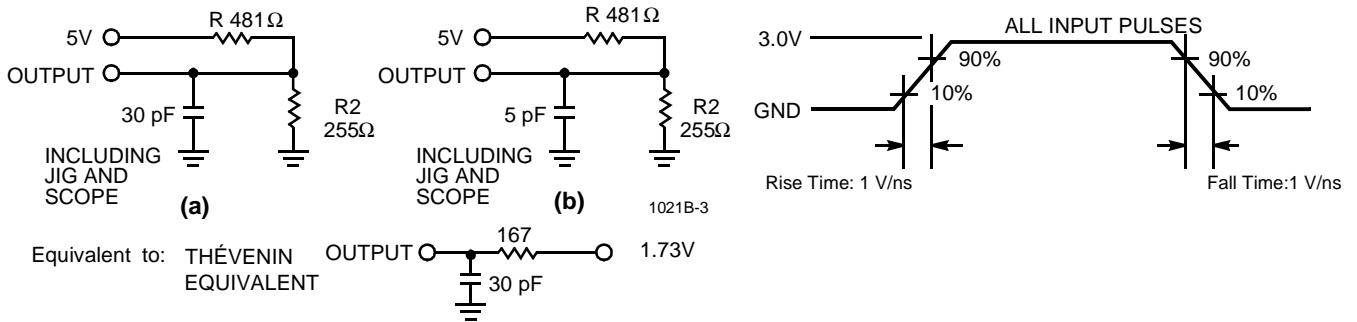
### Notes:

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

## Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

## AC Test Loads and Waveforms



### Notes:

4. Tested initially and after any design or process changes that may affect these parameters



## Switching Characteristics<sup>[5]</sup> Over the Operating Range

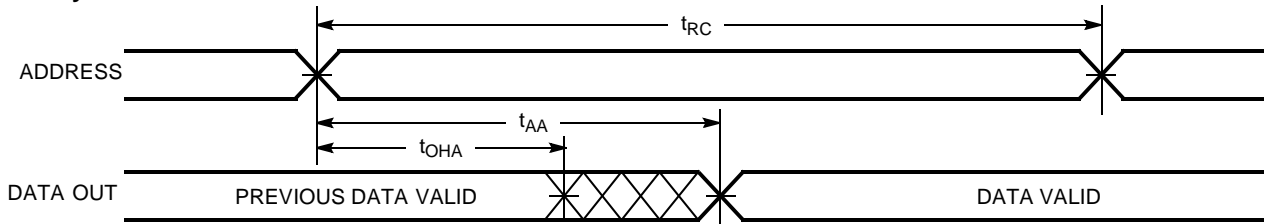
Parameter	Description	WCFS1016C1C 12ns		WCFS1016C1C 15ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	12		15		ns
t <sub>AA</sub>	Address to Data Valid		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		6		7	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		6		7	ns
<b>WRITE CYCLE<sup>[8]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7	ns
t <sub>BW</sub>	Byte Enable to End of Write	8		9		ns

### Notes:

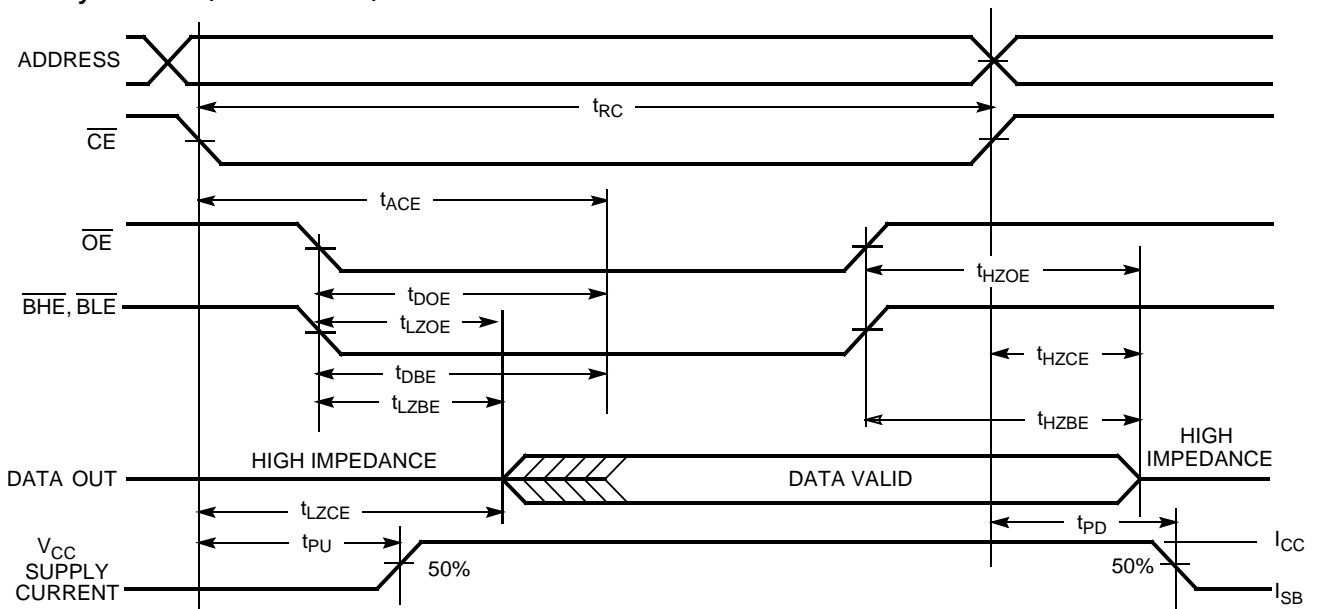
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
6. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
7. t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and BHE / BLE LOW.  $\overline{CE}$ ,  $\overline{WE}$  and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1<sup>[9, 10]</sup>



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>

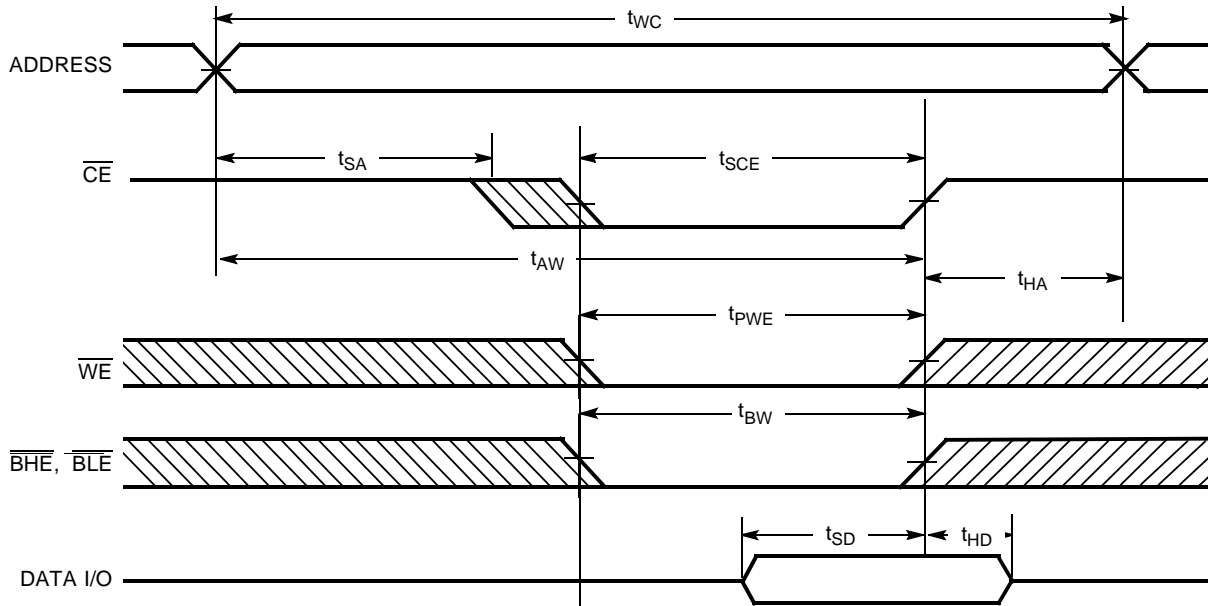


Notes:

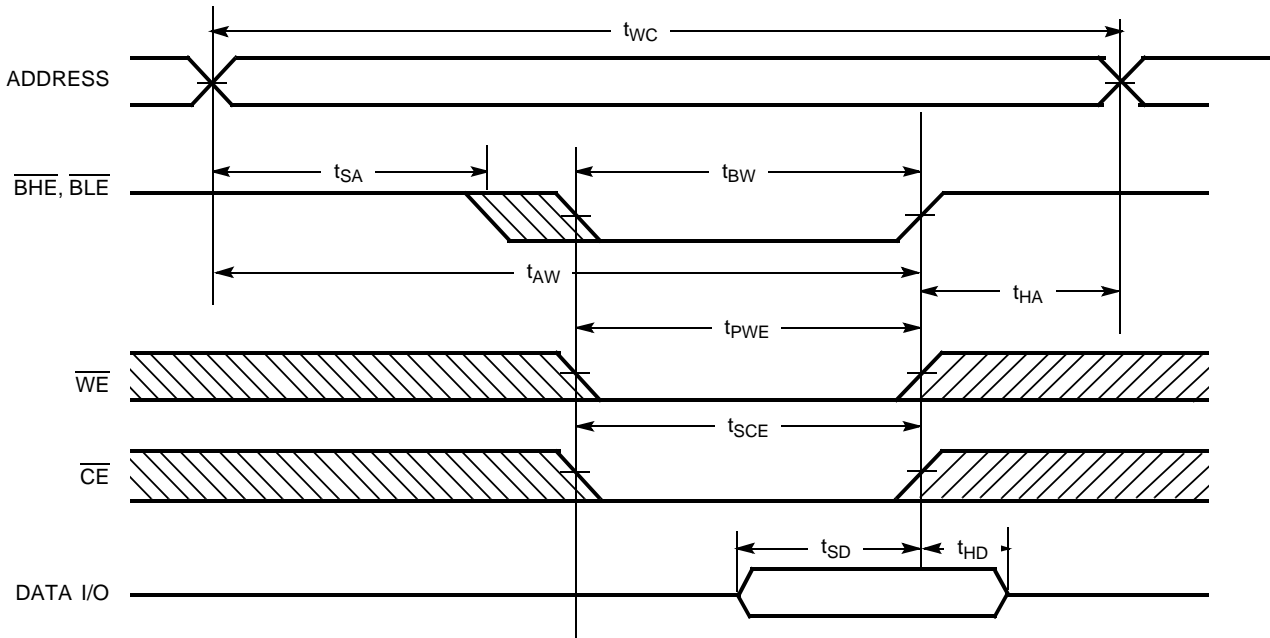
- 9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE} = V_{IL}$ .
- 10.  $\overline{WE}$  is HIGH for read cycle.
- 11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) <sup>[12, 13]</sup>



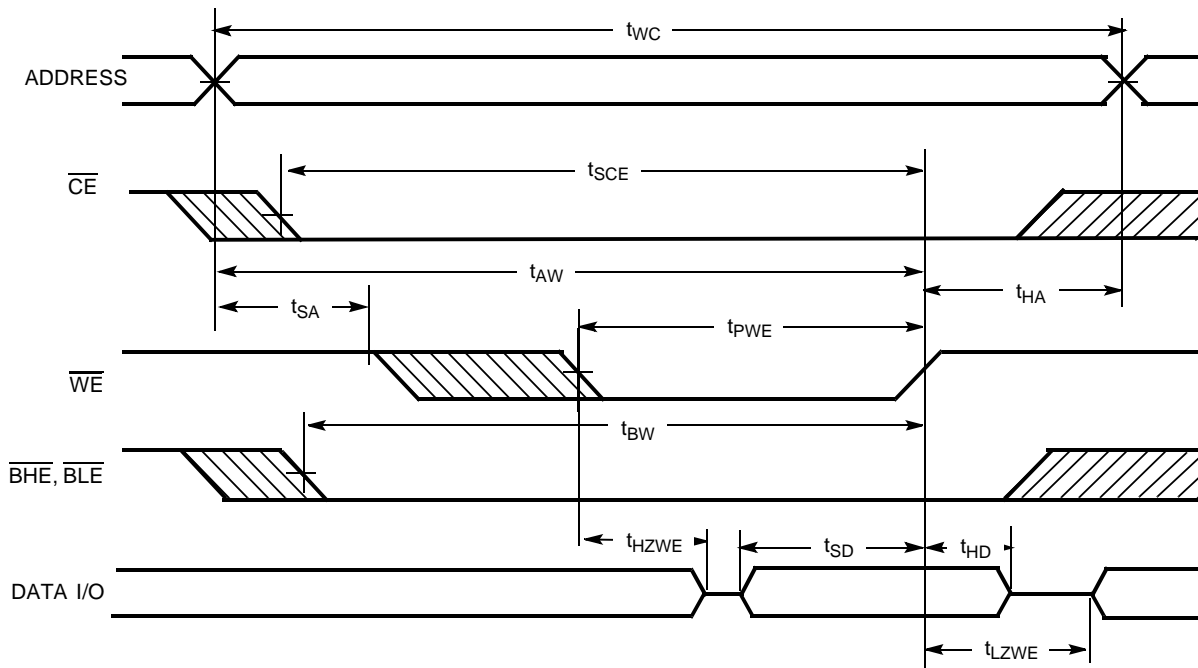
Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



Notes:

12. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled, LOW)**

**Truth Table**

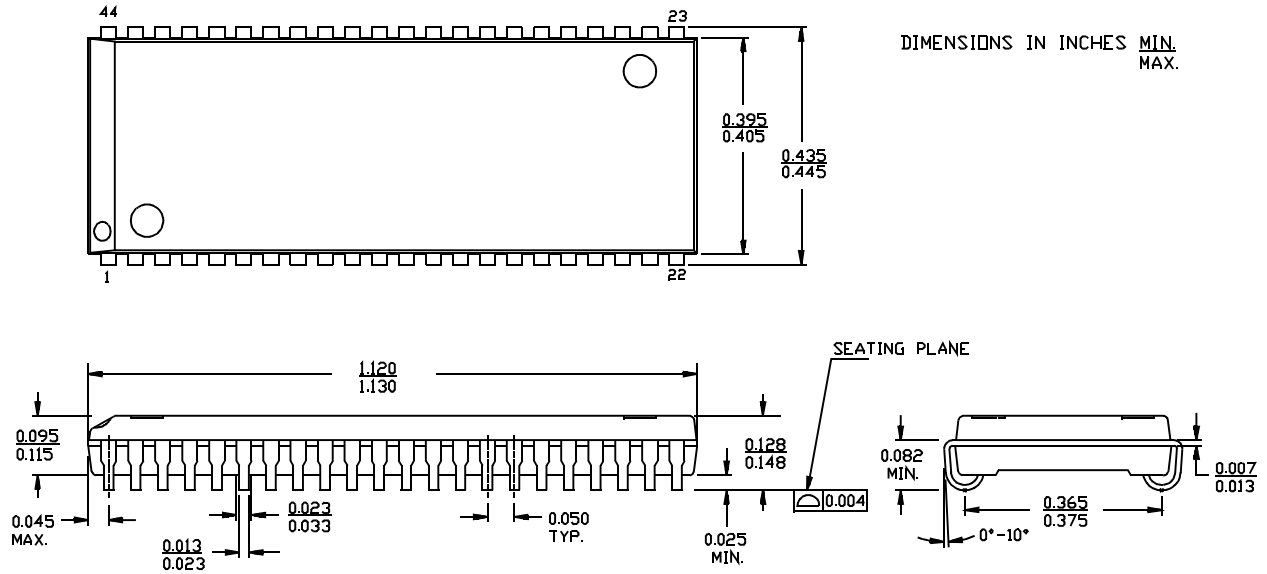
CE	OE	WE	BLE	BHE	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	WCFS1016C1C-JC12	J	44-Lead (400-Mil) Molded SOJ	Commercial
15	WCFS1016C1C-JC15	J	44-Lead (400-Mil) Molded SOJ	

Package Diagrams

44-Lead (400-Mil) Molded SOJ J







<b>Document Title: WCFS1016C1C 64K x 16 Static RAM</b>			
<b>REV.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	4/15/02	XFL	New Datasheet